Graduate School of Information Sciences / School of Engineering

Computer Architecture Laboratory (Prof. Kobayashi)

Inventing Next-Generation Computing Systems and Exploiting their Potentials through Application Development

What is Computer Architecture?
Structure of computers and their control methods

Toward Smart Architecture covering Cellphones to Supercomputers!

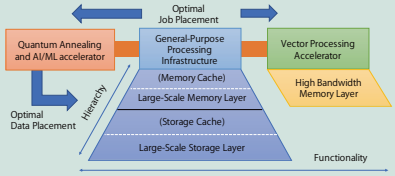
We accept your questions from our website. Please visit the following URL and contact us.

https://www.cal.is.tohoku.ac.jp/

Our laboratory aims at establishing elemental hardware technologies for next-generation computing systems and developing high-performance applications and its optimization technologies. We are also focusing on computer architectures in the Post-Moore's era, which integrate conventional computing technologies with new information processing technologies such as quantum annealing and artificial intelligence. Moreover, we are conducting research about high-performance infrastructures and applications that can fulfill the potentials of the new computer architectures, and their social deployments.

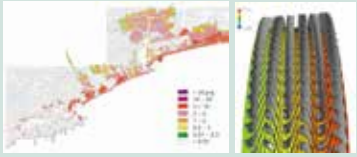
Quantum Annealing Assisted Supercomputing Systems

Quantum annealing (QA), which can effectively solve combinatorial problems, has attracted attention. This research focuses on the integration of QA technologies into conventional computing as a single system image, and development and deployment of their killer applications: a real-time tsunami inundation simulation with routing assistance for evacuation.



Acceleration of Science and Engineering Simulations

One of the requirements of a safe and secure society is to realize faster science and engineering simulations. This research aims at improving the simulation performance using various kinds of computer systems.



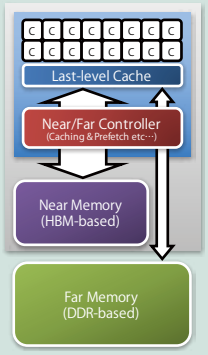
Examples of Science and Engineering Simulations
(Tsunami Inundation Forecast and Flow around a Turbine)

Vector Supercomputer (photo from NEC)

Hardware Accelerator (photo from intel.com)

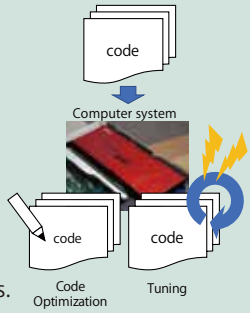
Near/Far Memory Systems for Next-Generation Computing Systems

A modern computer needs a memory system with a high performance and a large capacity. The goal of this research is to achieve a Near/Far memory system that consists of memory modules with different performances and capacities. Moreover, the system appropriately organizes the application data among these modules by data access characteristics.



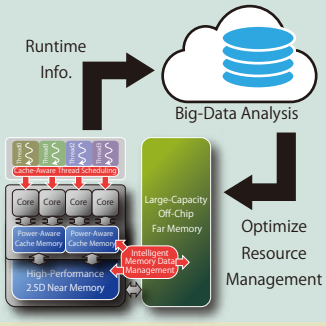
Code Optimization and Tuning to Exploit Potentials of Microprocessors

Microprocessors increase diversity due to the trends in manufacturing technologies and applications. This research evaluates various latest microprocessors and, based on the evaluation results, adopts the applications to the microprocessors by optimizing and tuning the application codes to obtain the high performances.



Resource Usage Optimization by Machine Learning

Since a microprocessor executes billions of instructions in one second, its runtime log data becomes significantly large. This research regards these data as "Big Data" and analyzes them by using machine learning. The analyzed results are used to optimize the management of hardware resources, such as cache memories.



Cache Memories by Different Memory Devices

Cache memories occupy a large part of a microprocessor, and their energy consumptions need to be reduced. This research solves the problem by using new memory devices for the cache memories and by optimizing the data management on the cache memories with the different memory devices without degrading the performances.